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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/813,464	03/30/2004	Thomas Aaron Winslow	18039L	4674

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EXAMINER	
CHOE, HENRY	

ART UNIT	PAPER NUMBER
2817	

DATE MAILED: 06/07/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/813,464	WINSLOW, THOMAS AARON	
	Examiner	Art Unit	
	Henry K. Choe	2817	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4-9,11-16,18,19,21,22 and 24-30* is/are rejected.

7)☒ Claim(s) *3, 10, 17, 20 and 23* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *9/24/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 2, 4-9, 11-14, 21, 22, 24-28 and 30 are rejected under 35 U.S.C. 102(b) as being anticipated by Dening et al [(Fig. 10) patent # 6,313,705].

Regarding claims 1, 8, 21, 27, 28 and 30, Dening et al (Fig. 10) discloses an amplifier circuit comprising a first transistor (Q2), a second transistor (Q1), a ballast resistor (R6) which is coupled between an emitter terminal (emitter of Q2) of the first transistor (Q2) and a base terminal (base of Q1) of the second transistor (Q1), a feedback stabilization circuit (R3) which is coupled to the first transistor (Q2), a diode stack circuit (Q4, Q5) which is coupled to the first transistor (Q2), one additional resistor (R2) which is coupled between the emitter terminal (emitter of Q2) of the first transistor (Q2) and a base terminal (base of Q2) of the first transistor (Q2), and wherein a control voltage (Vbias) applied to a base terminal (base of Q2) of the first transistor (Q2) controls the amplification of a signal applied to the base terminal (base of Q1) of the second transistor (Q1).

Regarding claims 2, 9 and 22, a biasing resistor (R1) which is coupled between a first input node (1002) and the base terminal (base of Q2) of the first transistor (Q2).

Regarding claims 4, 11 and 24, the diode stack circuit including two transistors (Q4, Q5).

Regarding claims 5, 12 and 25, one bypass capacitor (C1) which is coupled to the at least two transistors (Q4, Q5).

Regarding claims 6, 13 and 26, one bypass capacitor (C1) coupled to the first transistor (Q2).

Regarding claims 7 and 14, one additional resistor (R2) which is coupled between the emitter terminal (emitter of Q2) of the first transistor (Q2) and a base terminal (base of Q2) of the first transistor (Q2).

Claims 15, 16, 18, 19 and 29 are rejected under 35 U.S.C. 102(b) as being anticipated by Jarvinen (Fig. 2).

Regarding claims 15 and 29, Jarvinen (Fig. 2) discloses an amplifier circuit comprising a first transistor (Q2), a second transistor (Q1), a ballast resistor (a rectangle box located between an emitter of transistor Q2 and a base of transistor Q1) which is coupled between an emitter terminal (emitter of Q2) of the first transistor (Q2) and a base terminal (base of Q1) of the second transistor (Q1), one bypass capacitor (an output capacitor) which is coupled to a collector terminal (a collector of Q2) of the first transistor (Q2), and wherein a control voltage (Vbias) applied to a base terminal (base of Q2) of the first transistor (Q2) controls the amplification of a signal applied to the base terminal (base of Q1) of the second transistor (Q1).

Regarding claim 16, a biasing resistor (a rectangle box located between the bias voltage terminal and base of Q2) coupled between a first input node (bias voltage terminal) and the base terminal (base of Q2) of the first transistor (Q2).

Regarding claim 18, a diode stack circuit includes two transistors (Q3, Q4).

Regarding claim 19, one bypass capacitor (output capacitor) coupled to the two transistors (Q3, Q4).

Allowable Subject Matter

Claims 3, 10, 17, 20 and 23 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Patent numbers (6,882,227; 6,549,076) are the amplifier circuits with the bias circuits.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Henry Choe whose telephone number is (571) 272-1760.

HENRY CHOE
PRIMARY EXAMINER

#1019